Note on Si pixel readout

- # of channel ~ 3M (~ 400 chips * 8192 ch)
  → zero suppression at FEM desirable
- occupancy ~ 0.5% (1st layer, central)
  # of hits ~ 7000/event
- ~ 25 staves, 16 chips / stave
- read 8 chips from each side of a stave

ALICE1 chip performance

- see F. Meddi, NIM A465 (2001) 40-45 (http://doc.cern.ch/archive/electronic/cern/preprints/ali/ali-2000-003.pdf)
- clock speed 10 MHz max.
- readout: 25.6 us/chip (256 us/10 chips)
  → only one chip within 40 us (phenix limit)

Parallel readout plan

- read 8 chips in parallel
- 2 layers (horizontal + vertical) in ALICE
  → 8 layers (one for each chip)
- FEM recieves 32*8 inputs at 10 MHz
- FEM does zero-suppression
- Of course, we have to design FEM
- FEM at the end of a stave possible?
  (seemingly NO)

Zero suppression scheme

- Input: 256 inputs / 100 ns, 256 times.
- Almost all inputs are zero
- For all channels that are "1", output the addresses of the channels (16 bits).
- Plus some additional data (parity, header, trailer, ...) to satisfy PHENIX requirements
- Data amount: ~ 15 kB/event ← acceptable